

Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. **(Currently Amended)** An addition circuit for digital data with delayed saturation operation for the most significant digital bits, the circuit comprising:
 - a digital adder for the addition of digital input data values which are present at data inputs of the digital adder to form a summation output data value, which is output at an output of the digital adder, the data inputs having a predetermined data bit width n , and
 - a saturation circuit for limiting the summation output data value present at a data input of the saturation circuit within a data value range which is determined by an upper threshold data value and a lower threshold data value, the $n-m$ least significant data bits of the summation output data value being present directly with ~~the~~ a clock signal at the data input of the saturation circuit and the m most significant data bits of the summation output data value being switched through only with ~~the~~ an inverted clock signal proceeding the clock signal at the data input of the saturation circuit a clock-state-controlled latch register.
2. **(Original)** The addition circuit as claimed in claim 1, wherein input registers are provided for buffer-storing the digital input data values.
3. **(Original)** The addition circuit as claimed in claim 1, wherein an output register is provided for buffer-storing the summation output data value limited by the saturation circuit.
4. **(Currently Amended)** The addition circuit as claimed in claim 3, wherein the input registers and the output register are connected to a clock line for applying ~~[[a]]~~ the clock signal.

5. **(Original)** The addition circuit as claimed in claim 1, wherein the clock-state-controlled latch register has a control input, which is connected to the clock signal line via an inverter circuit.
 6. **(Original)** The addition circuit as claimed in claim 1, wherein the two threshold data values are settable.
 7. **(Original)** The addition circuit as claimed in claim 1, wherein the saturation circuit has a first comparator for comparing the present summation output data value with the upper threshold data value and a second comparator for comparing the present summation output data value with the lower threshold data value.
- 8- 14. **(Cancelled)**